CLAIMS

1. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first, second, and third inductors connected in series between a first input terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its other end connected to one end of said third inductor, said third inductor having its other end connected to said first common point;

a first resistor having its one end also connected to said first common point and its other end connected to a first output terminal;

fourth, fifth, and sixth inductors connected in series between a second input terminal and a second common point;

said four inductor having its one end connected to said second input terminal and its other end connected to one end of said fifth inductor, said fifth inductor having its other end connected to one end of said sixth inductor, said sixth inductor having its other end connected to said second common point;

a second resistor having its one end also connected to said second common point and its other end connected to a second output terminal; and

a capacitor having its one end connected to said first common point and its other end connected to said second common point.

2. An impedance blocking filter circuit as claimed in Claim 1, wherein said first and fourth inductors are comprised of ferrite toroids.

3. An impedance blocking filter circuit as claimed in Claim 2, wherein said second and fifth inductors have values on the order of 220 μH.

4. An impedance blocking filter circuit as claimed in Claim 3, wherein said third and sixth inductors have values on the order of 10 mH.

5. An impedance blocking filter circuit as claimed in Claim 4, wherein said first and second resistors have values on the order of 22 Ohms.

6. An impedance blocking filter circuit as claimed in Claim 5, wherein said capacitor has the value on the order of 22 nf.

7. An impedance blocking filter circuit as claimed in Claim 1, further comprising current limiting protection means connected between said common points and said output terminals for reducing current spikes caused by the customer's terminal equipment going off-hook.

8. An impedance blocking filter circuit as claimed in Claim 7, wherein said current limiting protection means is comprised of first and second depletion mode field-effect transistors and first and second transient protection varistors.

9. An impedance blocking filter circuit as claimed in Claim 8, wherein said first depletion mode field-effect transistor has its conduction path electrodes interconnected between said first common point and said one end of said first resistor and its gate electrode connected to said other end of said first resistor, said second depletion mode field-effect transistor having its conduction path electrodes interconnected between said second common point and said one end of said second resistor and its gate electrode connected to said other end of said second resistor, said first varistor having its one end connected also to said first common point and its other end connected to said first output terminal, said second varistor having its one end connected also to said second common point and its other end connected to said second output terminal.

10. An impedance blocking filter circuit used in telecommunication systems for interconnecting between incoming telephone lines and customer's terminal equipment so as to unconditionally block impedances from above 20 KHz due to the customer's terminal equipment from an ADSL network unit and/or home networking interface unit, said filter circuit comprising:

first, second, and third inductors connected in series between a first input terminal and a first common point;

said first inductor having its one end connected to said first input terminal and its other end connected to one end of said second inductor, said second inductor having its other end connected to one end of said third inductor, said third inductor having its other end connected to said first common point;

a seventh inductor and a first resistor connected in series between said first common point and a first output terminal, said seventh inductor having its one end connected also to said first common point and its other end connected to one end of said first

resistor, said first resistor having its other end connected to a first output terminal;

fourth, fifth, and sixth inductors connected in series between a second input terminal and a second common point;

said four inductor having its one end connected to said second input terminal and its other end connected to one end of said fifth inductor, said fifth inductor having its other end connected to one end of said sixth inductor, said sixth inductor having its other end connected to said second common point;

an eighth inductor and a second resistor connected in series between said second common point and a second output terminal, said eighth inductor having its one end connected also to said second common point and its other end connected to one end of said second resistor, said second resistor having its other end connected to a second output terminal; and

45 a capacitor having its one end connected to said first common point and its other end connected to said second common point.

11. An impedance blocking filter circuit as claimed in Claim 10, wherein said first and fourth inductors are comprised of ferrite toroids.

12. An impedance blocking filter circuit as claimed in Claim 11, wherein said second and fifth inductors have values on the order of 220 μH.

13. An impedance blocking filter circuit as claimed in Claim 12, wherein said third and sixth inductors have values on the order of 5-10 mH.

14. An impedance blocking filter circuit as claimed in Claim 13, wherein said seventh and eighth inductors have values on the order of 5-10 mH.

15. An impedance blocking filter circuit as claimed in Claim 14, wherein said first and second resistors have values on the order of 22 Ohms.

16. An impedance blocking filter circuit as claimed in Claim 15, wherein said capacitor has the value on the order of 47 nf.

17. An impedance blocking filter circuit as claimed in Claim 1, further comprising home network demarcation filter means interconnected between the incoming telephone lines and internal house wiring for blocking the impedance of the customer's terminal equipment from home networking signals.

18. An impedance blocking filter circuit as claimed in Claim 17, said demarcation filter means is comprised of six inductors and two capacitors.

19. An impedance blocking filter circuit as claimed in Claim 10, further comprising home network demarcation filter means interconnected between the incoming

telephone lines and internal house wiring for blocking the impedance of the customer's terminal equipment from home networking signals.

20. An impedance blocking filter circuit as claimed in Claim 19, said demarcation filter means is comprised of six inductors and two capacitors.